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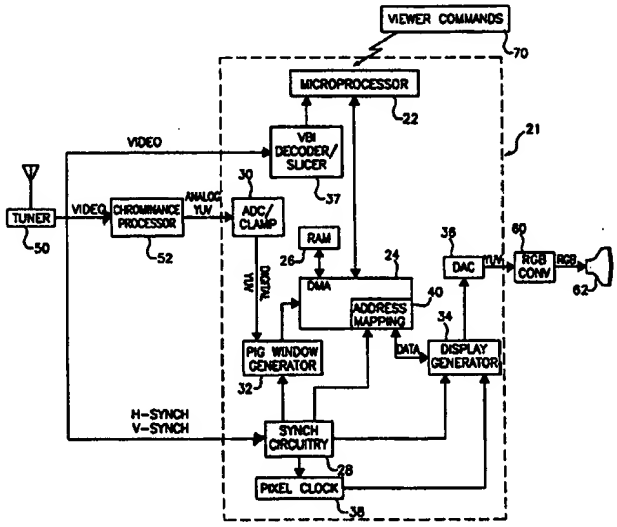
(54) Title: PICTURE-IN-GUIDE GENERATOR



(57) Abstract

A picture-in-guide generator (21) has an output adapted to drive a display monitor (62) and an input adapted to receive a television signal. A display generator (34) feeds drive signals to the output in synchronism with the display monitor (62). EPG information is extracted from the television signal and stored in memory (26). The pixel size of the television signal is reduced. The reduced pixel size television signal is stored in memory (26). The EPG data and the television signal are retrieved from memory (26) and stored in the display generator (34). The EPG data and the television signal are fed from the display generator (34) to the output in a continuous data stream ordered to produce a picture-in-guide display (10) on the monitor (62). Preferably, the picture-in-guide generator (21) is implemented on a single integrated circuit chip.

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PICTURE-IN-GUIDE GENERATOR

CROSS-REFERENCE TO RELATED APPLICATION

This application claims priority of U.S. Application No. 60/072,428, filed on January 26, 1998, the disclosure of which is incorporated fully herein by reference.

BACKGROUND OF THE INVENTION

The disclosures of the following patent applications are incorporated fully herein by reference: Application No. 08/475,395 filed June 7, 1995; International Application WO96/07270; Application No. 60/053,330 filed July 21, 1997; Application No. 60/061,119 filed October 6, 1997; and Application No. 60/055,237 filed August 12, 1997. Also incorporated by reference is the publication entitled "The CTC140 Picture in Picture System (CPIP) Technical Training Manual" available from Thomson Consumer Electronics, Inc., Indianapolis, IN.

An electronic program guide (EPG) provides a television viewer with updatable television schedule information in the form of an on-screen graphical display. The EPG may provide scheduling information for current and future broadcast programs as well as summaries of television program content for a particular program.

One particularly convenient format for an EPG is a picture-in-guide (PIG) display. A PIG display includes a real-time video image of a tuned television program displayed in a small window inset in a larger graphic guide. The PIG display provides many options to the viewer. The viewer may continue to view the television program s/he was watching before entering the guide while browsing through the television scheduling information in the guide. Alternatively, the program displayed in the PIG window may change to correspond to a selected channel in the guide as the viewer cursors through program listings in the guide. The viewer may also pull up the PIG display to find out more information about the program s/he is currently watching, such as start/stop time or a program synopsis, while continuing to view the program in the inset PIG window.

Typically, a PIG EPG display is produced using an EPG generator, which includes a microprocessor, a vertical blanking interval (VBI) decoder/slicer, an on-screen display generator, a digital-to-analog converter (DAC), synchronization (synch) circuitry, and a memory on one chip, and a separate chip including a picture-in-picture (PIP) generator, a DAC, synch circuitry, and microprocessor interface circuitry.

The PIP generator uses two video signals to create a big background picture and a small inset picture. The small picture is generated by decimating a subordinate video signal, e.g., by writing one out of every three pixels on one out of every three lines into a video

memory. A composite display having the big picture in the background and the small picture as an inset is generated by scanning the big picture normally and then using a high speed switch to scan the small picture image from the video memory when the scanner reaches the PIP window area on the screen of the display monitor. Thus, the high speed switch must operate at the scan line frequency of the display monitor.

However, for a PIG display, it is unnecessary to provide two real-time video images since the main display comprises textual and graphical information, e.g., a program guide, and not a real-time, moving video image. The high speed switch of the PIP is relatively expensive. Also, using separate chips for the EPG generator and PIP generator requires more components and is more difficult to integrate into consumer electronics components such as televisions, VCR's, satellite receivers, or the like.

It is therefore desirable to consolidate the components necessary to provide a PIG display into one chip.

SUMMARY OF THE INVENTION

A picture-in-guide generator has an output adapted to drive a display monitor and an input adapted to receive a television signal. A display generator feeds drive signals to the output in synchronism with the display monitor. EPG information is extracted from the television signal and stored in memory. The pixel size of the television signal is reduced. The reduced pixel size television signal is stored in memory. The EPG data and the television signal are retrieved from memory and stored in the display generator. The EPG data and the television signal are fed from the display generator to the output in a continuous data stream ordered to produce a picture-in-guide display on the monitor. Preferably, the picture-in-guide generator is implemented on a single integrated circuit chip.

DESCRIPTION OF THE DRAWINGS

The features of specific embodiments of the best mode contemplated of carrying out the invention are illustrated in the drawings, in which:

FIG. 1 illustrates a program guide display in a picture-in-guide (PIG) format;

FIG. 2 is a schematic of a PIG generator according to one embodiment of the invention;

FIG. 3 is a schematic of the organization of data in RAM according to one embodiment of the invention;

FIG. 4 is a schematic representation of the Y U V components of a standard color bar video signal; and

FIG. 5 is a schematic of an analog-to-digital conversion and clamping circuitry according to one embodiment of the invention.

DETAILED DESCRIPTION OF A SPECIFIC EMBODIMENT

According to the invention, a picture-in-graphics (PIG) generator is provided for producing a PIG display on a television screen or computer monitor. There are generally two display types available in a television system using a PIG generator. The first type is a full-screen video display comprising a real-time image of a broadcast television program. The second type, a PIG display, includes background graphics and a real-time video image in a small inset window.

FIG. 1 illustrates a PIG display 10 of an electronic program guide (EPG) comprising a graphics portion 12 and a picture window 14. The picture window 14, hereafter referred to as the PIG window, contains a video image of the television program displayed in the full-screen video display, but in reduced size, generally reduced by a factor of three in both width and height, i.e., 1/9 the size of the screen. Another possible screen for display in a PIG system is a full-screen graphics display.

The graphics portion 12 of the PIG display 10 takes up a majority of the screen. The graphics portion generally includes text, icons, and background graphics of several different colors. The graphics may include highlighting of text or sections of the screen. In an EPG system, the viewer can generally navigate through different guides without changing the television program displayed in the PIG window 14. In some EPG systems, when the viewer places a cursor 16 on a different channel designation 18 or program title 20 in the graphics portion, the system automatically tunes the associated tuner 50 to the selected channel and displays the program broadcast on that channel in the PIG window 14.

According to a preferred embodiment of the invention, the components necessary to generate a PIG display 10 are provided on a single chip to be incorporated into televisions, VCR's, stand-alone units, satellite receivers or the like. By providing all the components on a single chip, the overall package size can be reduced as well as the overall gate count and bus interface size of that chip.

FIG. 2 is a schematic of the components of a preferred embodiment of the invention provided on a single chip 21. These include a microprocessor 22, a memory controller or direct memory access (DMA) device 24, a random access memory (RAM) 26, synchronization regenerating (synch) circuitry 28, analog-to-digital conversion (ADC) and clamping circuitry 30, a PIG window generator 32, a display generator 34, and digital-to-analog conversion (DAC) circuitry 36.

The microprocessor 22 receives raw text data, e.g., EPG data, from a data source and stores the raw text data in the RAM 26. For example, EPG data may be embedded in the vertical blanking interval (VBI) of the television signal received by television tuner 50 and extracted by a VBI decoder/slicer 37. Preferably, the RAM 26 has a storage capacity of 4Mbit or greater, and includes a data RAM 31 for storing text data and video RAM (VRAM) 31 for storing video data, as well as free space for use as working space 35 between the data RAM 31 and VRAM 33, as shown in FIG. 3. The microprocessor 22 organizes data storage in the RAM 26 and can assign addresses for both text data and video data. However, the microprocessor 22 is relatively slow compared to the video processing hardware, e.g., the PIG window generator 32 and display generator 34. Accordingly, the microprocessor 22 generally processes only addressing data and text data, and not video data. The microprocessor is in two-way communication with the DMA 24. The microprocessor 22 communicates with the DMA 24 to access the RAM 26 via both a data bus and an address bus.

Preferably, there is only one RAM. This RAM 26 is accessed by three different components: the microprocessor 22, the PIG window generator 32, and the display generator 34. This places a high access load on the RAM as all three components may vie for access to the RAM simultaneously. However, only one sample of so many bits may be accessed per access cycle, for example 8 bits for a 516KX8bit RAM. A multiplexing device is necessary to resolve the arbitration between the components. Accordingly, the microprocessor 22, PIG window generator 32 and the display generator 34 each access the RAM through the DMA 24. The DMA 24 is a multiplexing and arbitrating circuit that facilitates sharing of the RAM 26 by switching access between the three components in turn. The DMA 24 includes buffer memories to temporarily store data input from out-of-turn components between access cycles. The DMA 24 stores text data and video data in the correct address in the RAM 26 and then retrieves the appropriate data from a selected address from the RAM when needed.

As stated above, the RAM 26 preferably has 4Mbit or greater storage capacity and is subject to a high access loading. One way to accommodate for the high access load and to transfer the data faster is to select a 256KX16bit RAM rather than an 512KX8bit RAM in order to allow the DMA 24 to sample more information, i.e., 16 bits, per access cycle instead of 8 bits. The system receives a video signal from the tuner 50. Horizontal and vertical (h- and v-) synchronization signals are split from the video signal and routed to the synch circuitry 28. The synch circuitry includes a pixel clock 28. The pixel clock determines the x- and y-coordinates of each pixel to be displayed on the screen. The y-coordinate corresponds to the scan line number of the screen, and the x-coordinate corresponds to the pixel number in each scan line.

The video portion of the input video from the tuner 50 is converted to a Y U V analog video signal by chrominance processor 52 in the television. This is an intermediate signal conversion commonly used in television systems between the input video and RGB signal displayed on the cathode ray tube (CRT) 62.

FIGS. 4A, 4B, and 4C illustrate the Y U V components 54, 56, 58, respectively, of a standard color bar video signal. Component 54 is the luminance (Y) signal with a horizontal sync pulse 55. Component 56 is the chrom-signal (-V). Component 58 is the back porch region of the chroma-signal (-U) for video clamping. Each component of the signal is converted to a digital form by the ADC/clamp circuitry 30, illustrated in more detail in FIG. 5. The clamping portion of the ADC/clamping circuitry 30 reduces distortion in the signal due to, for example, low frequency noise and dc bounce when switching the signal.

The PIG window generator 32 receives the digital Y U V video signals corresponding to the full screen video image. The PIG window generator 32 reduces the overall picture size by decimating the video data before sending it to the DMA 24 for storage in the VRAM. To decimate the video data, the PIG window generator 32, in cooperation with the synch circuitry 28, selects, for example, one out of every three pixels and one out of every three scan lines, i.e., a 1:3 ratio, and then sends this data to the DMA 24 for storage in VRAM 33. Other decimation ratios are possible., e.g., 1:4, in order to generate different sized PIG windows.

The correct address for storing the video data from PIG window generator 32 in the VRAM 33 is determined by address mapping circuitry 40 which is preferably incorporated into the DMA 24. Using the synch signal from the synch circuitry 28 and the pixel clock 38, the address mapping circuitry 40 stores video data corresponding to each pixel on the CRT in an appropriate address site in the VRAM for later access for display. This process is generally referred to as "bit mapping."

The display generator 34 includes a graphics generator which formats fonts for the text to be displayed, icons, color and highlighting, and background graphics for the graphics portion 12 of the PIG display 10. The graphics data is routed to the address mapping circuitry 40 which, in cooperation with the DMA 24, stores the video data in address sites in the VRAM 33 corresponding to pixel coordinates on the screen.

Generation of the PIG display 10 (FIG. 1) according to the preferred embodiment will now be explained.

In response to a viewer command device 70, e.g., an IR remote, for a given PIG EPG display, the microprocessor 22 accesses the appropriate text data for that display from the raw text data in the data RAM 31. The microprocessor 22 configures the text data for display and

routes the text data, with appropriate addresses for display of the text, to the DMA 24 for storage in the VRAM 33.

All video data for generating the PIG display 10, including the text and graphics of the graphics portion 12, and the video image of the PIG window 14, is stored in the VRAM 33 as described above. The display generator 34, in cooperation with the address mapping circuitry 40 and synch circuitry 28, accesses the pre-organized contents of the VRAM to create an image for display on the screen of the CRT 62. The data for each pixel to be displayed on the screen is stored in the VRAM 33 with an address corresponding to the x- and y-coordinate of that pixel on the screen. The display generator 34 accesses the appropriate data from the VRAM 33 for each pixel in sequence as determined by the pixel clock 38 using the synch signals from the synch circuitry 28. This synch signal is generated by the synch circuitry 28 from the h- and v-synch signals in the input video.

Although it is preferable to store the entire screen field or frame in VRAM 33 at one time in bit mapped fashion, less than the entire screen, i.e., only part of the screen, could be stored at one time and the display processing could in effect be executed in pixel groups that are smaller than the entire screen.

The display generator 34 converts the digital Y U V signals for each pixel and outputs them to the DAC circuitry 36 in a continuous data stream in proper order to produce a picture-in-guide display similar to that shown in FIG. 1 on the screen of CRT 62. The DAC circuitry converts the data to analog Y U V video signals. These analog Y U V video signals are then converted to analog RGB signals by RGB conversion circuitry 60 in the television prior to being displayed on the screen of the CRT 62.

In an alternative embodiment of the invention, RAM 30 is located "off chip" where it is connected by a data bus to DMA 24.

Tuner 50, chrominance processor 52, RGB converter 60, CRT 62, and viewer commands 70 are part of the television apparatus. In other words, these components serve the dual function of helping to display the television signal in conventionally in a full screen format and to display the picture-in-guide format. The other components are unique to the picture-in-guide format.

The design of the PIG circuitry according to the present invention on a single chip 21 provides a more economical package with a reduced size and gate count. The invention reduces overall gate count by requiring only a single gate array for each of the microprocessor 22, synch circuitry 28, DAC circuitry 36, and DMA 24, instead of two gate arrays for each of these components on separate PIP and EPG chips as used in known television systems to generate a PIG display. It should also be noted that display generator 34 feeds both picture information and EPG information to CRT 62 under the control of pixel

clock 38 and synch circuitry 28 in a continuous stream of data. Thus, a video (i.e., moving picture) image is created in an EPG display without a high speed switch.

The described embodiment of the invention is only considered to be preferred and illustrative of the inventive concept; the scope of the invention is not to be restricted to such embodiment. Various and numerous other arrangements may be devised by one skilled in the art without departing from the spirit and scope of this invention. For example, separate RAM's could be used to store the EPG data and the reduced size television signal. Further, the invention could be used in a digital television transmission system as well, in which case the ADC, DAC, and VBI slicer could be eliminated.

WHAT IS CLAIMED IS:

1. A picture-in-guide generator comprising:

an output adapted to drive a display monitor;

a display generator that feeds drive signals to the output in synchronism with the display monitor;

an input adapted to receive a television signal;

means connected to the input for extracting EPG information from the television signal;

means for storing the EPG information in memory;

means for reducing the pixel size of the television signal;

means for storing the reduced pixel size television signal in memory;

means for retrieving the EPG data and the television signal from memory;

means for storing the retrieved EPG data and the television signal in the display generator; and

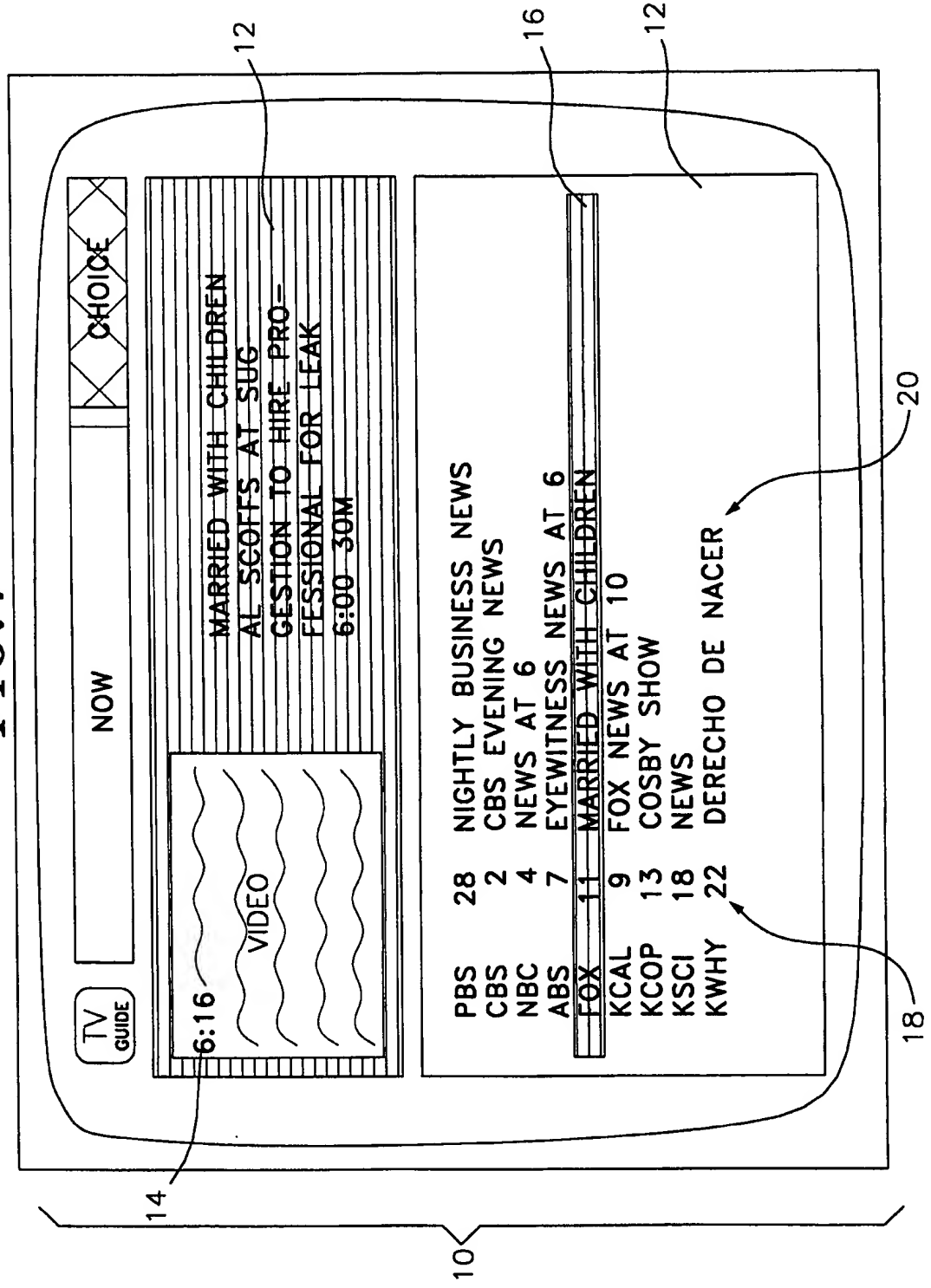
means for feeding the EPG data and the television signal from the display generator to the output in a continuous data stream ordered to produce a picture-in-guide display on the monitor.

2. The picture-in-guide generator of claim 1, implemented in a single integrated circuit chip.

3. The picture-in-guide generator of claim 2, in which the extracting means is a VBI decoder.

4. The picture-in-guide generator of claim 3, in which the memory comprises one or more RAM's.

FIG. 1


TV GUIDE
NOW
CHOICE
6:16
VIDEO
MARRIED WITH CHILDREN
AL SCOFFS AT SUG
GESTION TO HIRE PRO-
FESSIONAL FOR LEAK
6:00 30M
PBS 28 NIGHTLY BUSINESS NEWS
CBS 2 CBS EVENING NEWS
NBC 4 NEWS AT 6
ABS 7 EYEWITNESS NEWS AT 6
FOX 11 MARRIED WITH CHILDREN
KCAL 9 FOX NEWS AT 10
KCOP 13 COSBY SHOW
KSCI 18 NEWS
KWHY 22 DERECHO DE NACER
10
12
12
14
16
18
20

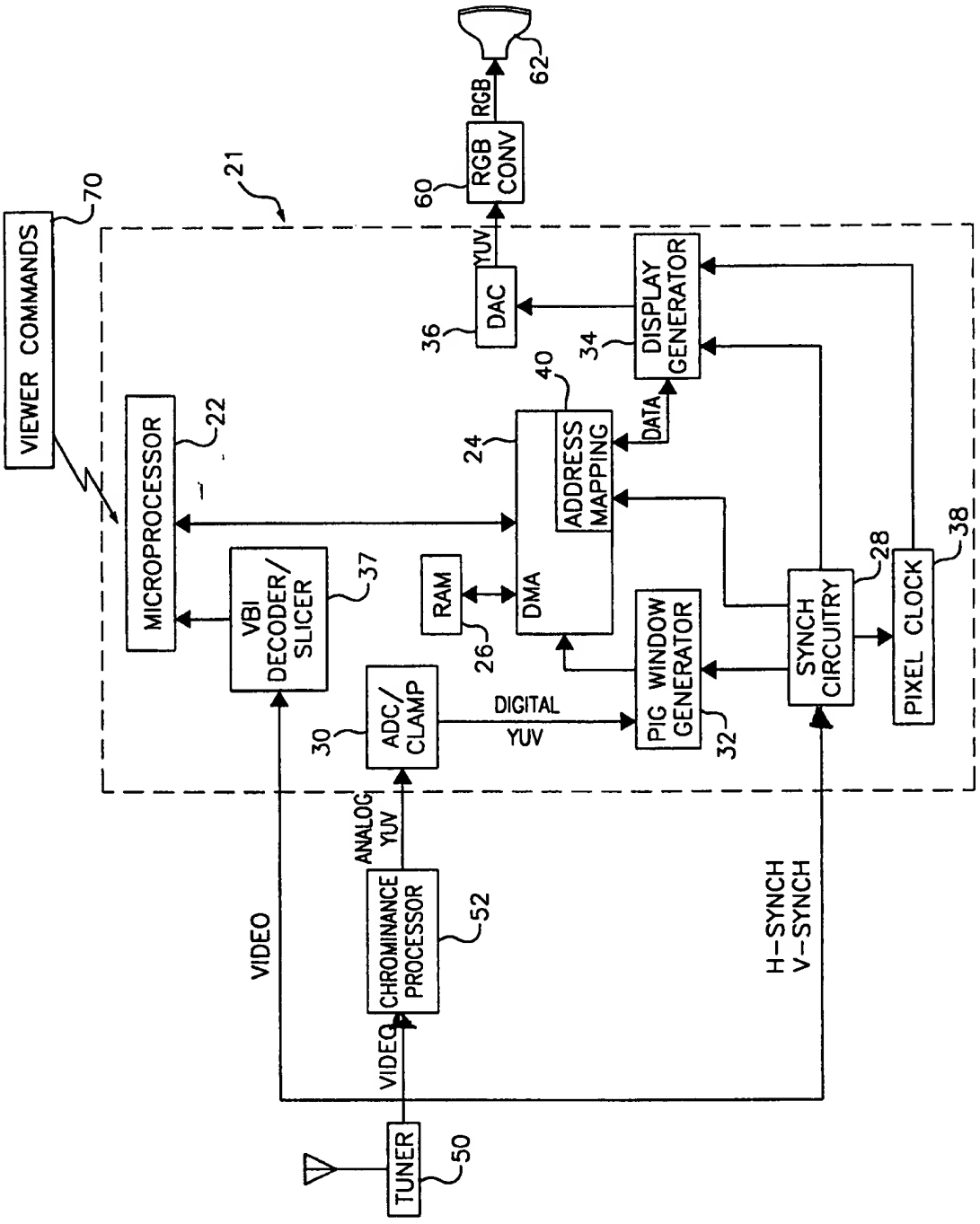

VIEWER COMMANDS
70
21
MICROPROCESSOR
22
VBI DECODER/ SLICER
37
RAM
26
DMA
24
ADDRESS MAPPING
40
DATA
DISPLAY GENERATOR
34
DAC
36
YUV
RGB CONV
60
RGB
62
ADC/ CLAMP
30
DIGITAL YUV
PIG WINDOW GENERATOR
32
SYNCH CIRCUITRY
28
PIXEL CLOCK
38
ANALOG YUV
CHROMINANCE PROCESSOR
52
VIDEO
VIDEO
TUNER
50
H-SYNCH
V-SYNCH

FIG.2

FIG.3

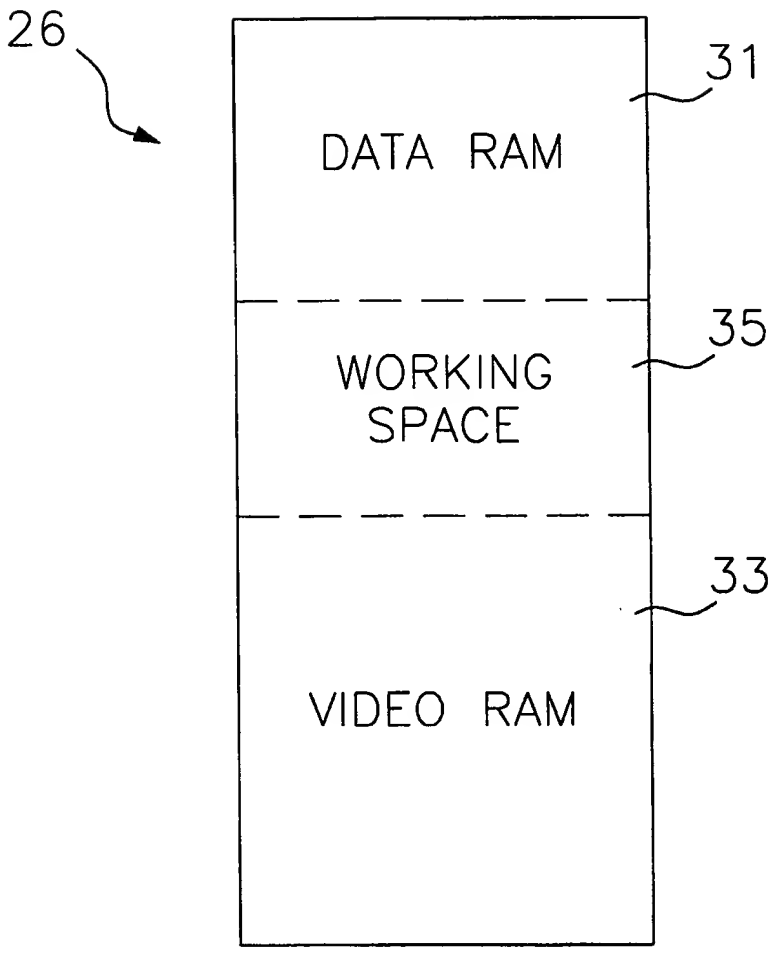


FIG. 4A

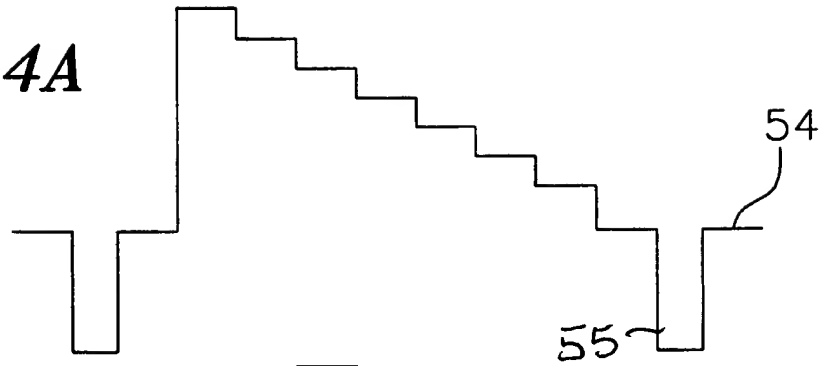


FIG. 4B

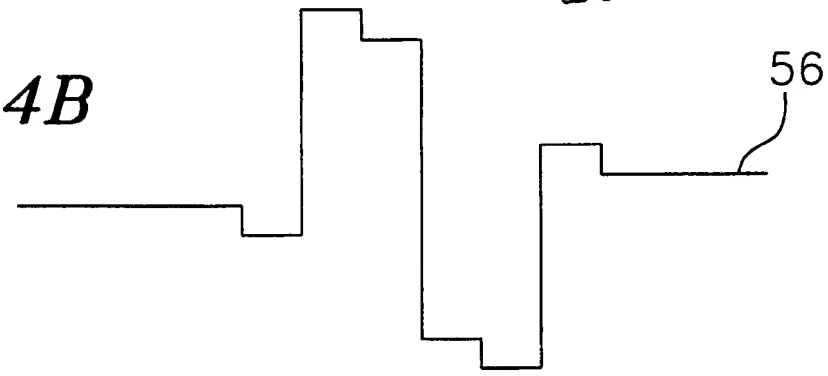
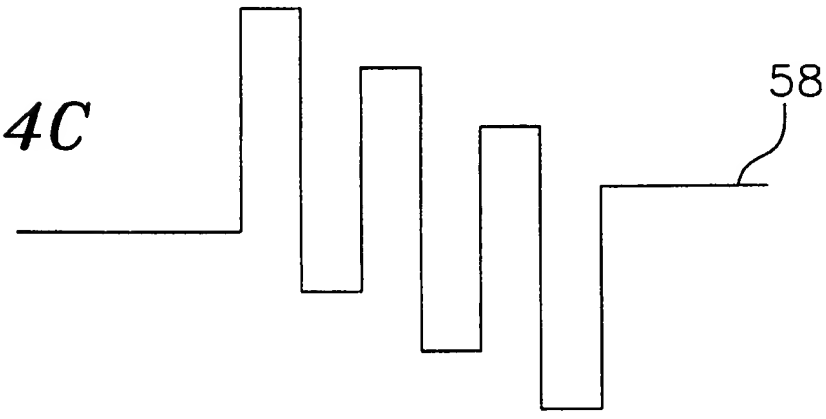


FIG. 4C



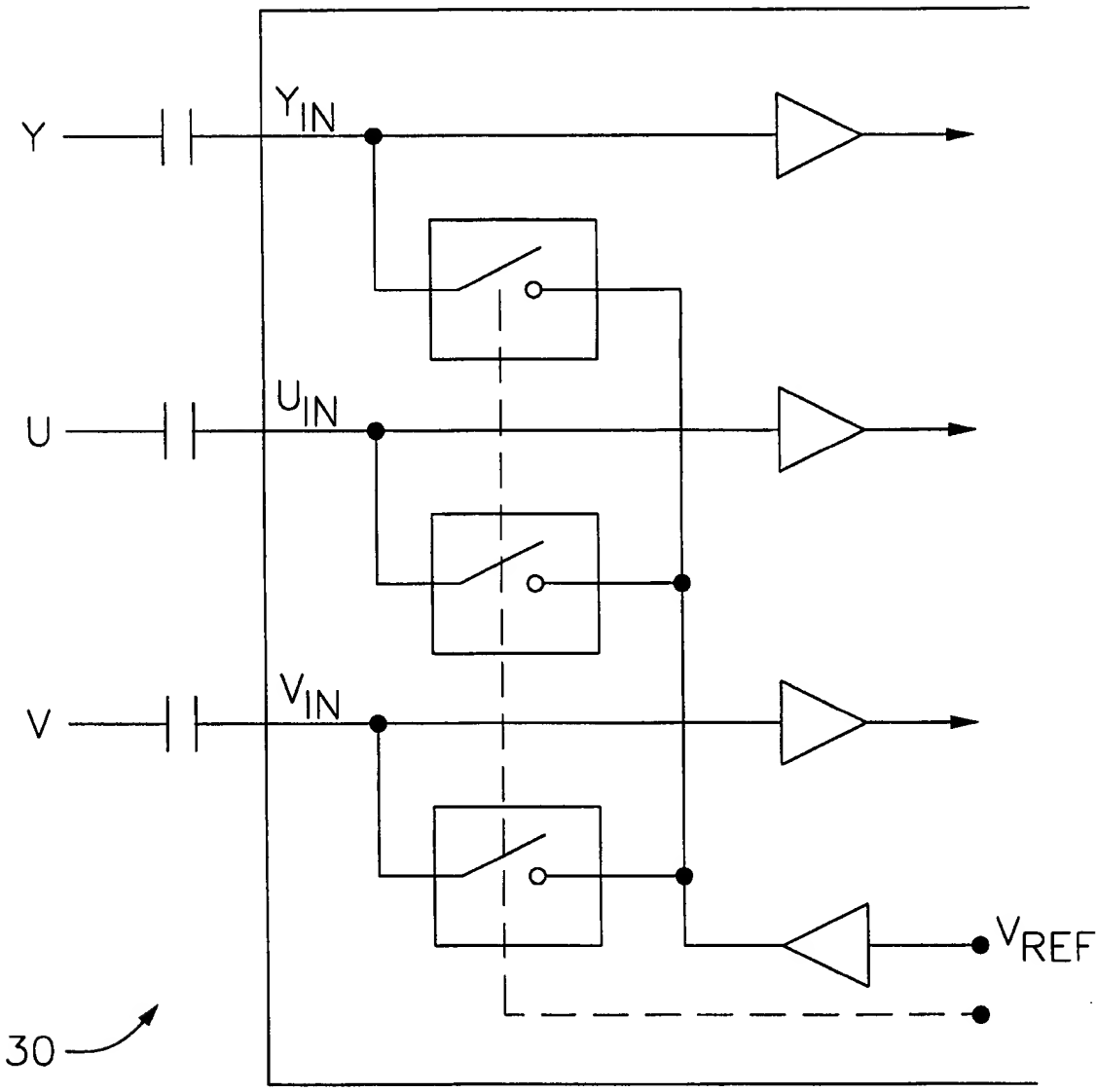


FIG.5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/01906

A. CLASSIFICATION OF SUBJECT MATTER
IPC(6) :H04N 5/50, 5/445
US CL : 348/569, 906, 564
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 348/569, 906, 564, 565, 563, 566, 567, 568, 589, 600
H04N 5/50, 5/445

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X,P	US 5,828,419 A (BRUETTE et al.) 27 October 1998, Fig. 1 and accompanying text.	1-4
X,P	US 5,809,204 A (YOUNG et al) 15 September 1998, Fig. 22A and accompanying text.	1-4

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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